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APPL NUM 10076920	FILING DATE 02/15/2002	CLASS 209	SUBCLASS	GAU 3653	EXAMINER
**APPLICANTS: Deliwala Shrenik;					
**CONTINUING DATA VERIFIED: THIS APPLICATION IS A DIV OF 09/991,542 11/10/2001 WHICH IS A CIP OF 09/859,693 05/17/2001 AND CLAIMS BENEFIT OF 60/293,615 05/25/2001 AND CLAIMS BENEFIT OF 60/297,208 06/08/2001					
** FOREIGN APPLICATIONS VERIFIED:					
PG-PUB	DO NOT PUBLISH <input type="checkbox"/>	RESCIND <input type="checkbox"/>			
Foreign priority claimed <input type="checkbox"/> yes <input type="checkbox"/> no 35 USC 119 conditions met <input type="checkbox"/> yes <input type="checkbox"/> no Verified and Acknowledged Examiners's initials				ATTORNEY DOCKET NO 53168-500301D3	
TITLE : Integrated optical/electronic circuits and associated methods of simultaneous generation thereof					
<small>U.S. DEPT. OF COMM./PAT. & TM.-PTO-435L (Rev. 12-94)</small>					

NOTICE OF ALLOWANCE MAILED		Assistant Examiner	CLAIMS ALLOWED		
			Total Claims		Print Claim for O.G
ISSUE FEE		Primary Examiner	DRAWING		
Amount Due	Date Paid		Sheets.Drwg.	Figs.Drwg.	Print Fig.
<input type="checkbox"/> TERMINAL DISCLAIMER		PREPARED FOR ISSUE	Application Examiner		
		WARNING: The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368, Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.			

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